REMARKS

Applicants request entry of the above amendment and allowance. In response to the office action of February 16, 2005 and the notice of non-compliant amendment mailed June 2, 2005, claims 20-26 are added and claim 14 is amended to correct a grammatical error.

Submitted with this amendment are revised drawings to correct errors in the drawings as filed. The specification supports the revised drawings. The specification discloses the following process steps:

> Turning to FIG. 6, the screen oxide layer 125 is removed and a metal layer 220 of platinum or titanium is deposited on the upper surface of the epitaxial layer 124. The metal layer 220 is heated to 650.degree. C. and then to 850.degree. C. to form a highly conductive silicide layer on the surface of the source regions 114. The metal reacts with the underlying silicon in the epitaxial layer to form a metal silicide 225. That layer is also formed over the surface of the polysilicon 112 in the trench. The metal does not react with the oxide 116 on the trench wall. The unreacted metal 220 is removed by an etch step that leaves the silicide layer 225 but removes the unreacted metal 220. The surface portion of the polysilicon in the trenches is also silicided. Those skilled in the art may use one or more processes and other metals for forming the silicide layer 225. The conductive silicide layer reduces the RDSON resistance of the source region. Because silicide it is highly conductive, only a relatively small area of the silicided source region is needed to provide a reliable electrical contact. As such, one may cover the entire surface of the epitaxial layer with an insulating material and open vias in the insulating material to contact the silicide layer 225.

That process shows that unreacted metal is removed before the insulating layer is applied over the silicided source and silicided gate. Removing the unreacted metal leaves the ends of the trench oxide exposed. However, the drawings as filed show a continuous layer over the source. The new drawings show the silicide layer over the source and the trench polysilicon but not over the end of the trench insulating layer at the top of the trench adjacent to the source.

Claim 14 was rejected under 35 USC § 102 (b) on grounds that each and every element of the claim is shown in Davari (US 4881105) reference. That rejection is clearly erroneous. The vias in the Davari reference to not extend to the highly conductive

source layer. Davari shows not vias to that layer. Instead, all the vias in Davari extend to the conductive trench material. As such, the Davari reference fails to show or suggest a distinguishing feature of claim 14.

The invention of claim 14 allows the maker of a device to reduce the space between adjacent source regions, overcome defects associated with source etching and eliminated critical alignment steps of large vias. Now the vias to the source can be smaller because the source is silicided and the silicided source is protected against damage during etching steps and is more conductive by virtue of the silicide layer.

The Davari reference does not show or suggest the features of claim 20 where the top of the trench polysilicon is a reacted metal, in particular a silicide (claim 22).

Davari does not bring an insulating layer into contact with the tops or ends of the trench insulating layer. Thus, claim 25 is patentable over Davari.

Claim 26 adds further limitation to the vias introduced in claim 14. Those vias terminate on the highly conductive source layer and electrically contact the conductive material in the vias.

Having thus distinguished the claims from the applied art of record, reconsideration and allowance are requested.

Respectfully submitted,

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